CLAIM LISTING

1. (Previously Presented) A video request manager comprising:

a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; and

a second state machine for commanding a memory controller to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels.

2. (Original) The video request manager of claim 1, wherein the second state machine commands the memory controller to write the second portion, such that a resource contention occurs between the command to fetch reference pixels, and the command to write the second portion.

3. (Original) The video request manager of claim 2, wherein the second state machine commands the memory controller to write the second portion, such that the command to fetch reference pixels is given priority during the resource contention.

4. (Cancelled).

5. (Currently Amended) A circuit for decoding video data, said circuit comprising:

a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture;

a motion compensator for decoding another portion of the picture;

a video request manager comprising:

a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; and

a second state machine for issuing a command to write a second portion of the picture;

a memory controller for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

6. (Cancelled).

7. (Previously Presented) The circuit of claim 5, wherein the memory controller further comprises:

an arbiter for causing the memory controller to give priority to the command to fetch the reference pixels.

8. (Previously Presented) The circuit of claim 5, wherein the memory controller further comprises:

a write buffer for storing the second portion of the picture while fetching the reference pixels.

9. (Original) The circuit of claim 8, wherein the memory controller writes the second portion of the picture from the write buffer to a memory system, after fetching the reference pixels.

10-14. (Cancelled).

15. (Previously Presented) The video request manager of claim 1, wherein the second state machine loads the memory controller with the second portion reconstructed from decoding while the memory controller fetches the reference pixels.